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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,482	09/21/2004	Peter J. Geiss	BUR920040004US1	5481

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EXAMINER	
BUDD, PAUL A	
ART UNIT	**PAPER NUMBER**
2815	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/711,482	GEISS ET AL.	
	Examiner	Art Unit	
	Paul A. Budd	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *16-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/27/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I claims **1-15** in the reply filed on 11 January is acknowledged and appreciated.

Specification

2. The disclosure is objected to because of the following informalities:

On page 5, line 5 of [Para 22], change "(Ph)" to - -(P)- -.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims **1-5,** and **8** are rejected under 35 U.S.C. 102(b) as being anticipated by Endo el al. (US Patent 5,177,583).

Regarding claim **1,** Endo teaches a heterojunction bipolar transistor comprising:

a semiconductor substrate [FIG. 1, 101, column 11, lines 45-47] of a first conductivity type [p] including a collector region [FIG. 1; 102, 103, 104; column 11, lines 49-55];

a base region [FIG. 1; 105, 106; column 11, lines 55-61] formed on said substrate [101];

an emitter region [FIG. 1; 107, 108; column 11, lines 62-68] formed over said base region [105, 106]; and

at least one of said collector [103 ($5x10^{16}$), 104 ($4x10^{17}$); col 11 lns 50-54], base [105 ($5x10^{17}$), 106 ($1x10^{19}$); col 11, lns 57-61] and emitter [107 ($5x10^{17}$), 108 ($1x10^{20}$); col 11, lns 62-68] regions including a first region doped with an impurity having a first concentration [shown in parenthesis above] and a second region doped with said impurity having a second concentration [shown in parenthesis above].

Regarding claim **2,** Endo teaches the heterojunction bipolar transistor of claim **1**, wherein said base region comprises SiGe [FIG. 1, 105, 106; column 11, lines 55-61].

Regarding claim **3,** Endo teaches the heterojunction bipolar transistor of claim **1**, wherein said first concentration is less than said second concentration [bases 105 ($5x10^{17}$), 106 ($1x10^{19}$)].

Regarding claim **4,** Endo teaches the heterojunction bipolar transistor of claim **1**, wherein said emitter region [FIG. 1; 107 ($5x10^{17}$), 108 ($1x10^{20}$)] comprises said first [107 ($5x10^{17}$)] region doped with a dopant [Sb, Antimony] having a first concentration [$5x10^{17}$] and said second region [108 ($1x10^{20}$)] doped with said dopant [Sb, Antimony] having a second concentration [$1x10^{20}$] greater than said first concentration [$5x10^{17}$].

Regarding claim **5,** Endo teaches the heterojunction bipolar transistor of claim **4**, wherein said first region [107] is formed closer [See FIG. 1] to an emitter-base junction region than said second region [108].

Regarding claim **8,** Endo teaches the heterojunction bipolar transistor of claim **1**, wherein an impurity concentration profile of said first or second regions comprises a step profile [See FIG. 2, step profile] or a graded profile.

4. Claims **1-3** are rejected under 35 U.S.C. 102(e) as being anticipated by Sadovnikov (US Patent 6,967,144).

Regarding claim **1,** Sadovnikov teaches a heterojunction bipolar transistor comprising:

a semiconductor substrate [col 2, lines 35] of a first conductivity type [n] including a collector region [FIG. 3; 302; col 2, lines 302];

a base region [FIG. 3, 304] formed on said substrate;

an emitter region [FIG. 3, 306] formed over said base region [304]; and

at least one of said collector, base [304] and emitter regions including a first region [304a] doped with an impurity [boron] having a first concentration [col 2, lines 37-46; "1E18"] and a second region [304b] doped with said impurity [boron] having a second concentration [col 2, lines 37-44;"highly p-doped (e.g. boron epitaxial SiGe", "1E19"].

Regarding claim **2,** Sadovnikov teaches the heterojunction bipolar transistor of claim **1**, wherein said base region comprises SiGe [column 2, line 38].

Regarding claim **3,** Sadovnikov teaches the heterojunction bipolar transistor of claim **1**, wherein said first concentration [1E18] is less than said second concentration [1E19].

5. Claims **1-15** are rejected under 35 U.S.C. 102(e) as being anticipated by Toyoda et al. (US Patent 7,135,721).

Regarding claim **1,** Toyoda teaches a heterojunction bipolar transistor comprising:

a semiconductor substrate [FIG. 2, 10, col 6, lines 40-41] of a first conductivity type [p] including a collector region [FIG. 2, 11; col 6, lines 41-45];

a base region [FIG. 2, 12 & 13; col 6, lines 45-68] formed on said substrate [10];

an emitter region [FIG. 2; 15 & 14a; col 7, lines 5-22] formed over said base region [12, 13]; and

at least one of said collector, base [FIG. 2; 12, 13] and emitter regions including a first region [13] doped with an impurity [Carbon] having a first concentration [col 6, lines 46-47, "low C content"] and a second region [12] doped with said impurity [Carbon] having a second concentration [col 6, lines 44-45, "high C content"]

Regarding claim **2,** Toyoda teaches the heterojunction bipolar transistor of claim **1**, wherein said base region comprises SiGe [col 6, lines 42-47, "SiGeC"].

Regarding claim **3,** Toyoda teaches the heterojunction bipolar transistor of claim **1**, wherein said first concentration is less than said second concentration [col. 6, lines 57-60].

Regarding claim **4,** Toyoda teaches the heterojunction bipolar transistor of claim **1**, wherein said emitter region [FIG. 2; 14a, 15] comprises said first [14a] region doped with a dopant [col 7, line 11; arsenic or phosphorus] having a first concentration [less than $1x10^{20}$] and said second region [15] doped with said dopant [col 7, line 11; arsenic or phosphorus] having a second concentration [$1x10^{20}$] greater than said first concentration [(somewhat less than $1x10^{20}$, col 7 lines 14-16, "This n-type impurity is diffused into the Si cap layer 14 by heat treatment, to form emitter region 14a in the SI cap layer 14"; Because of "Ficks Law" and thermodynamics the layer 14a MUST inherently have a concentration lower that its source of dopant=layer 15)].

Regarding claim **5,** Toyoda teaches the heterojunction bipolar transistor of claim **4**, wherein said first region [14a] is formed closer [See FIG. 2] to an emitter-base junction region than said second region [15].

Regarding claim **6,** Toyoda teaches the heterojunction bipolar transistor of claim **1**, wherein said base region [FIG. 2; 12, 13] comprises said first region [13] doped with a non-dopant [carbon] having a first concentration [col 6, lines 46-47, "low C content"] and said second region [12] doped with said non-dopant [carbon] having a second concentration [col 6, lines 44-45, "high C content"] greater than said first concentration [col. 6, lines 57-60].

Regarding claim **7,** Toyoda teaches the heterojunction bipolar transistor of claim **6**, wherein said first region [13] is formed closer [see FIG. 2] to an emitter-base junction region than said second region [12].

Regarding claim **8,** Toyoda teaches the heterojunction bipolar transistor of claim **1**, wherein an impurity concentration profile of said first or second regions comprises a step profile [See FIG.s 3A, 4A, 4B, 5A, 6A, 7A] or a graded profile. [These figures show both abrupt and graded profiles for at least one layer]

Regarding claim **9,** Toyoda teaches a heterojunction bipolar transistor comprising:

a semiconductor substrate [FIG. 2, 10, col 6, lines 40-41] of a first conductivity type [p] including a collector region [FIG. 2, 11; col 6, lines 41-45];

a base region [FIG. 2, 12 & 13; col 6, lines 45-68] formed on said substrate [10] including a first base region [13] doped with a non-dopant [carbon] having a first concentration [col 6, lines 46-47, "low C content"] and a second base region [12] doped with said non-dopant [carbon] having a second concentration [col 6, lines 44-45, "high C content"]; and

an emitter region [FIG. 2; 14a, 15] formed over said base region [12, 13] including a first emitter region [14a] doped with a dopant [col 7, line 11; arsenic or phosphorus] having a first concentration [as above, less than $1x10^{20}$ by thermal diffusion] and a second emitter region [15] doped with said dopant [arsenic or phosphorus] having a second concentration [$1x10^{20}$].

Regarding claim **10,** Toyoda teaches the heterojunction bipolar transistor of claim **9**, wherein said base region comprises SiGe [col 6, lines 42-47, "SiGeC"].

Regarding claim **11,** Toyoda teaches the heterojunction bipolar transistor of claim **9**, wherein said first base region [13] and said first emitter region [14a] are formed closer to an emitter- base junction region than said second base region [12] and said second emitter region [15].

Regarding claim **12,** Toyoda teaches the heterojunction bipolar transistor of claim **9**, wherein said non-dopant comprises carbon [col 6, lines 44-65].

Regarding claim **13,** Toyoda teaches the heterojunction bipolar transistor of claim **11**,wherein said first carbon concentration is from about $8x10^{18}$ cm^{-3} to about $5x10^{19}$ cm^{-3}, and said second carbon concentration is from about $1.5x10^{19}$ cm^{-3} to about $7x10^{19}$ cm^{-3}. This is evidenced by Toyoda's: 1) Claim 1, column 11, lines 20-23 where the applicants ranges are taught by the equation $Si_{1-x-y}Ge_xC_y$ ($0<x<1$, $\mathbf{0\leq y<1}$), 2) Toyoda's FIG. 1 where a continuum of x and y values are taught, 3) In column 4, lines 6-8, where Toyoda teaches "The carbon content of the portion of the base region adjacent to the emitter region may be 0.01% or more" (0.01% times silicon's density of $5x10^{22}$ cm^{-3} equals $5x10^{18}$ cm^{-3} which results in anticipating the applicant's claimed range by teaching $5x10^{18}$ cm^{-3} or more, 4) teaching on column 6, lines 61-63 that "The C content of at least the boundary portion of the second base region on the side of the emitter region should be *less than* 0.8%" which results in 0.8% times $5x10^{22}$ cm^{-3} equals $4x10^{20}$ cm^{-3} which includes the applicant's range where Toyoda teaches a range of greater than $5x10^{18}$ cm^{-3} and less than $4x10^{20}$ for the applicant's second concentration. The applicants claimed ranges are well known in the art as evidenced by Toyoda as well as others such as Sato (US Pat. Pub. 2004/0201461) on page 9, sections 0131, 0133, 0142, and figures 2, 3, 5, and 6. The applicant's choice of concentrations are an optimization of known ranges in the art and are dependent on the Boron concentration chosen for the base layer as evidenced by Toyoda or as Sato also points out.

Regarding claim **14,** Toyoda teaches the heterojunction bipolar transistor of claim **9**, wherein said dopant comprises arsenic [col 7, line 11; arsenic or phosphorus].

Regarding claim **15,** Toyoda teaches the heterojunction bipolar transistor of claim **14**, wherein said first arsenic concentration is from about $5x10^{19}$ cm^{-3} to about $3x10^{20}$ cm^{-3} [(somewhat less than $1x10^{20}$, col 7 lines 14-16, This n-type impurity is diffused into the Si cap layer 14 by heat treatment, to form emitter region 14a in the SI cap layer 14"; Because of "Ficks Law" and thermodynamics the layer 14a MUST have a concentration lower that its source of dopant=layer 15)], and said second arsenic concentration is from about $1x10^{20}$ cm^{-3} to about $7x10^{20}$ cm^{-3} [col 7, line 14, "$1x10^{20}$"].

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Sato et al. (US Pat. Pub. 2003/0201461). Also see the attached 892 form for this pertinent art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A. Budd whose telephone number 571-272-8796. The examiner can normally be reached on Monday to Friday 8:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JEROME JACKSON
PRIMARY EXAMINER